

WHAT IS CLAIMED

1           1. For use with a communication system in which a  
2 data packet is to be multicast to a plurality of  
3 recipients, a method of buffering and controllably  
4 supplying said data packet for delivery to multiple ones of  
5 a plurality of output ports associated with said recipients  
6 comprising the steps of:

7           (a) storing said data packet in only a single data  
8 packet storage location of a data packet buffer;

9           (b) storing, in a content-addressable memory, a  
10 plurality of respectively different address pointer words,  
11 each address pointer word containing a respectively  
12 different key field that is used to identify one of said  
13 plurality of output ports, and an address field that  
14 identifies said single data packet storage location of said  
15 packet buffer in which said data packet is stored;

16           (c) coupling a key to said respectively different key  
17 fields of said respectively different address pointer words  
18 stored in said content addressable memory, so as to access  
19 contents of the address field of an address pointer word  
20 whose key field matches said key;

21           (d) reading said data packet from said single data  
22 packet storage location of said packet buffer in accordance  
23 with said address field contents accessed in step (c); and

24           (e) coupling said address field contents accessed in  
25       step (c) to the address fields of said respectively  
26       different address pointer words stored in said content-  
27       addressable memory to determine whether said single data  
28       packet storage location of said data packet buffer is  
29       available to store a new data packet.

1           2.    A method according to claim 1, wherein steps (d)  
2       and (e) are conducted during a common memory cycle for said  
3       content-addressable memory.

1           3.    A method according to claim 1, wherein step (e)  
2       comprises generating a signal representative whether or not  
3       said accessed address field contents are contained in the  
4       address field of another address pointer word.

1           4.    A method according to claim 1, wherein step (e)  
2       comprises generating a signal representative of the  
3       availability of said single data packet storage location of  
4       said packet buffer to store a new data packet, in  
5       accordance with whether or not said address of said data  
6       packet single storage location of said packet buffer is  
7       contained in another address pointer word stored in said  
8       content-addressable memory.

1           5. A method according to claim 1, wherein said  
2 content-addressable memory comprises a data bit storage  
3 cell having a data input through which a data bit is  
4 written into said data bit storage cell, a data output  
5 through which a data bit is read out of said data bit  
6 storage cell, and an address input through which said data  
7 bit storage cell is selectively accessed, and a data bit  
8 comparator coupled to said data bit storage cell and being  
9 configured to determine whether the data bit stored in said  
10 data bit storage cell matches a reference data bit during  
11 a read cycle for said data bit storage cell.

1           6. A method of interfacing data with a data memory  
2 comprising the steps of:

3           (a) storing said data in said data memory by:

4               (a1) writing said data into a storage location of  
5 said data memory, and

6               (a2) writing, into one or more respective storage  
7 regions of a content-addressable memory, one or more  
8 respective address pointer words, each of which includes a  
9 respective key field that is used to identify said data,  
10 and an address field that identifies the address of said  
11 storage location of said data memory;

12 (b) reading said data from said data memory by:

13 (b1) coupling a key to key fields of address  
14 pointer words stored in storage regions of said content-  
15 addressable memory, and accessing said address of said  
16 storage location of said data memory from the address field  
17 of an address pointer word whose key field contains said  
18 key;

19 (b2) reading said data from said storage location  
20 of said data memory in accordance with said address  
21 accessed in step (b1); and

22 (c) coupling said address accessed in step (b1) to  
23 said content-addressable memory, to determine whether said  
24 address of said storage location of said data memory is  
25 contained in another address pointer word stored in said  
26 content-addressable memory.

1 7. A method according to claim 6, wherein steps (b2)  
2 and (c) are conducted during a common memory cycle for said  
3 content-addressable memory.

1 8. A method according to claim 6, wherein step (c)  
2 comprises selectively making said storage location of said  
3 data memory available for storage of new data, in  
4 dependence upon whether or not said address of said storage  
5 location of said data memory is contained in another  
6 address pointer word stored in said content-addressable  
7 memory.

1           9. A method according to claim 6, wherein step (a)  
2 comprises writing, into plural storage regions of said  
3 content-addressable memory, a plurality of address pointer  
4 words, each of which contains a respectively different key  
5 field used to identify said data, and said address of said  
6 storage location of said data memory.

1           10. A method according to claim 6, wherein said  
2 content-addressable memory comprises a data bit storage  
3 cell having a data input through which a data bit is  
4 written into said data bit storage cell, a data output  
5 through which a data bit is read out of said data bit  
6 storage cell, and an address input through which said data  
7 bit storage cell is selectively accessed, and a data bit  
8 comparator coupled to said data bit storage cell and being  
9 configured to determine whether the data bit stored in said  
10 data bit storage cell matches a reference data bit during  
11 a read cycle for said data bit storage cell.

1           11. For use with a communication system in which  
2 packetized data is to be controllably multicast to a  
3 plurality of recipients in accordance with multicast  
4 criteria, an output port data distribution architecture for  
5 buffering and controllably supplying packetized data for  
6 delivery to multiple ones of a plurality of output ports  
7 associated with said recipients comprising:

8           a packet buffer containing a plurality of storage  
9 locations that store data packets intended for delivery to  
10 one or more of said plurality of output ports;

11           a content-addressable memory containing a plurality of  
12 storage regions that store respectively different address  
13 pointer words, each address pointer word containing a  
14 respectively different key field that is used to identify  
15 a data packet to be delivered to one of said plurality of  
16 output ports, and an address field that identifies the  
17 address of one of said plurality of storage locations of  
18 said packet buffer in which said data packet is stored; and

19           a packet buffer access controller, which is operative  
20 to couple a key to key fields of address pointer words of  
21 said plural storage regions of said content-addressable  
22 memory, and thereby access contents of the address field of  
23 an address pointer word whose key field contains said key,  
24 the accessed address field contents being coupled to read  
25 out a data packet stored in one of said plurality of  
26 storage locations of said packet buffer, said accessed  
27 address field contents being coupled to the address fields  
28 of address pointer words stored in said content-addressable

29 memory, and wherein said content-addressable memory is  
30 operative to output a signal representative whether said  
31 accessed address field contents are contained in the  
32 address field of another address pointer word stored in  
33 said content-addressable memory.

1 12. An output port data distribution architecture  
2 according to claim 11, wherein said content-addressable  
3 memory is operative to output a signal indicating whether  
4 or not said storage location of said packet buffer is  
5 available for storage of a new data packet, in accordance  
6 with whether or not said address of said storage location  
7 of said packet buffer is contained in, another address  
8 pointer word stored in said content-addressable memory.

1 13. An output port data distribution architecture  
2 according to claim 11, wherein said packet buffer access  
3 controller is operative to cause a data packet, that is to  
4 be multicast to multiple output ports, to be stored in a  
5 single storage location of said packet buffer, and to cause  
6 multiple address pointer words to be stored in said  
7 content-addressable memory, respective ones of said  
8 multiple address pointer words containing different key  
9 fields for respectively different ones of said multiple  
10 output ports, and the same address field that identifies  
11 the address of said single data packet storage location of  
12 said packet buffer storing said data packet to be  
13 multicast.

1           14. An output port data distribution architecture  
2 according to claim 11, wherein said content-addressable  
3 memory contains a plurality of storage regions that store  
4 respectively different address pointer words, a respective  
5 storage region containing a first plurality of content  
6 addressable memory cells, the contents of which are  
7 associated with a first field of a respective address  
8 pointer word that identifies data to be accessed from a  
9 storage location in said packet buffer, and a second  
10 plurality of content addressable memory cells, the contents  
11 of which are associated with a second field of said  
12 respective address pointer word that identifies the address  
13 of said storage location in said packet buffer.

1           15. An output port data distribution architecture  
2 according to claim 14, wherein respectively different  
3 address pointer words stored in multiple ones of said  
4 plurality of storage regions of said content addressable  
5 memory contain respectively different first fields  
6 associated with respectively different ones of multiple  
7 instances of accessing said data from said storage location  
8 in said packet buffer, and a common second field that  
9 identifies the address of said storage location in said  
10 packet buffer for each of said multiple instances of  
11 accessing said data from said storage location in said  
12 packet buffer.



1           16. An output port data distribution architecture  
2 according to claim 15, wherein each of said first plurality  
3 of content addressable memory cells is configured to  
4 compare contents stored therein with a packet access key  
5 associated with data to be accessed from said storage  
6 location in said packet buffer, and to selectively read out  
7 contents of said second plurality of content addressable  
8 memory cells to address said storage location in said  
9 packet buffer in accordance with whether or not said packet  
10 access key matches said contents of said first plurality of  
11 content addressable memory cells.

1           17. An output port data distribution architecture  
2 according to claim 16, wherein each of said plurality of  
3 storage regions is further configured to compare contents  
4 stored therein with said read out contents of said second  
5 plurality of content addressable memory cells to determine  
6 whether any other of said plurality of storage regions  
7 contains said common second field of said respective  
8 address pointer word that identifies said address of said  
9 storage location in said packet buffer.

1           18. An output port data distribution architecture  
2 according to claim 17, wherein a respective storage region  
3 of said content-addressable memory is configured to output  
4 a signal indicating whether or not said storage location of  
5 said packet buffer is available for storage of new data, in  
6 accordance with whether another of said plurality of  
7 storage regions contains said common second field of said  
8 respective address pointer word.

1           19. An output port data distribution architecture  
2 according to claim 11, wherein a respective one of said  
3 second plurality of content addressable memory cells  
4 comprises a data bit storage cell having a data input  
5 through which a data bit is written into said data bit  
6 storage cell, a data output through which a data bit is  
7 read out of said data bit storage cell, and an address  
8 input through which said data bit storage cell is  
9 selectively accessed, and a data bit comparator coupled to  
10 said data bit storage cell and being configured to  
11 determine whether the data bit stored in said data bit  
12 storage cell matches a reference data bit during a read  
13 cycle for said data bit storage cell.

1           20. For use with a communication system in which a  
2 data packet is to be multicast to a plurality of  
3 recipients, a method of buffering and controllably  
4 supplying said data packet for delivery to multiple ones of  
5 a plurality of output ports associated with said recipients  
6 comprising the steps of:

7           (a) storing said data packet to be multicast in only  
8 a single data packet storage location of a data packet  
9 buffer;

10           (b) storing, in a content-addressable memory, a  
11 plurality of respectively different address pointer words,  
12 containing respectively different first fields, associated  
13 with multicasting of said data packet to multiple ones of  
14 said plurality of output ports, and a common address field  
15 that identifies said single data packet storage location of  
16 said packet buffer in which said data packet to be  
17 multicast is stored;

18           (c) coupling respectively different keys to said  
19 respectively different first fields of said respectively  
20 different address pointer words stored in said content  
21 addressable memory, to read out contents of said common  
22 address field for application to said packet buffer, and  
23 thereby cause said data packet to be read out from said  
24 single data packet storage location of said packet buffer  
25 and multicast to said multiple ones of said plurality of  
26 output ports; and

27           (d) in the course of reading out said contents of  
28           said common address field for application to said packet  
29           buffer in step (c), coupling said contents of said common  
30           address field to address fields of all of the address  
31           pointer words stored in said content addressable memory, to  
32           determine whether said data packet has been multicast in  
33           accordance with each address pointer word stored in said  
34           content addressable memory.

1           21. An output port centric digital data management  
2           architecture for a high speed packet switch comprising a  
3           content addressable memory which stores address information  
4           for controlling multiple accesses to the same data packet  
5           stored in a single memory address of a data packet output  
6           buffer, to selectively read out therefrom said same data  
7           packet to a plurality of ports of the switch, said content  
8           addressable memory being configured to store respectively  
9           different buffer address pointer words that identify said  
10          same data packet to be delivered to selected ones of said  
11          plurality of switch output ports, and point to the address  
12          of said single storage location of said packet buffer.

1           22. An output port centric digital data management  
2           architecture according to claim 21, wherein a respective  
3           address pointer word of said content addressable memory  
4           contains a first field that identifies said same data  
5           packet, and a companion address field that points to the  
6           address of said single storage location of said data packet  
7           output buffer, and wherein said content addressable memory  
8           is operative, during a first portion of a search thereof,  
9           to couple a packet request key to first fields of all  
10          address pointer words stored therein, and to cause  
11          information associated with a matching first field to  
12          access said matching first field's companion address field,  
13          said accessed companion address field being employed during  
14          a second portion of said search to read out said data  
15          packet from said single storage location of said packet  
16          output buffer, and to also be simultaneously coupled to  
17          address fields of all the address pointer words stored in  
18          said content addressable memory, in response to which said  
19          content addressable memory outputs a signal indicating  
20          whether the accessed address field is contained in another  
21          address pointer word stored therein, and thereby whether  
22          the address of said single output packet buffer storage  
23          location is available to store a new packet.

1           23. A content-addressable memory having a plurality  
2 of storage regions that store respectively different  
3 address pointer words, a respective storage region  
4 containing:

5           a first plurality of content addressable memory cells,  
6 the contents of which are associated with a first field of  
7 a respective address pointer word that identifies data to  
8 be accessed from a storage location in a memory; and

9           a second plurality of content addressable memory  
10 cells, the contents of which are associated with a second  
11 field of said respective address pointer word that  
12 identifies the address of said storage location in said  
13 memory.

1           24. A content addressable memory according to claim  
2 23, wherein respectively different address pointer words  
3 stored in multiple ones of said plurality of storage  
4 regions of said content addressable memory contain  
5 respectively different first fields associated with  
6 respectively different ones of multiple instances of  
7 accessing said data from said storage location in said  
8 memory, and a common second field that identifies the  
9 address of said storage location in said memory for each of  
10 said multiple instances of accessing said data from said  
11 storage location in said memory.

1           25. A content addressable memory according to claim  
2           24, wherein each of said first plurality of content  
3           addressable memory cells is configured to compare contents  
4           stored therein with a data access key associated with data  
5           to be accessed from said storage location in said memory,  
6           and to selectively read out contents of said second  
7           plurality of content addressable memory cells to address  
8           said storage location in said memory, in accordance with  
9           whether or not there is a match between contents stored in  
10          said first plurality of content addressable memory cells  
11          and said data access key.

1           26. A content addressable memory according to claim  
2           25, wherein each of said plurality of storage regions is  
3           further configured to compare contents stored therein with  
4           said read out contents of said second plurality of content  
5           addressable memory cells, and to output a signal indicating  
6           whether or not said storage location of said memory is  
7           available for storage of new data, in accordance with  
8           whether or not another of said plurality of storage regions  
9           contains said common second field of said respective  
10          address pointer word that identifies said address of said  
11          storage location in said memory.

1           27. A content addressable memory according to claim  
2           23, wherein a respective one of said second plurality of  
3           content addressable memory cells comprises a data bit  
4           storage cell having a data input through which a data bit  
5           is written into said data bit storage cell, a data output  
6           through which a data bit is read out of said data bit  
7           storage cell, and an address input through which said data  
8           bit storage cell is selectively accessed, and a data bit  
9           comparator coupled to said data bit storage cell and being  
10          configured to determine whether the data bit stored in said  
11          data bit storage cell matches a reference data bit during  
12          a read cycle for said data bit storage cell.

1           28. A content-addressable memory comprising an array  
2           of storage regions that store multibit words, each storage  
3           region being formed of a first plurality of content  
4           addressable memory cells, the contents of which are  
5           associated with a first field of a respective multibit  
6           word, and a second plurality of content addressable memory  
7           cells, the contents of which are associated with a second  
8           field of said respective multibit word, and wherein  
9           respectively different words stored in multiple ones of  
10          said plurality of storage regions of said content  
11          addressable memory contain respectively different first  
12          fields, and a common second field.



1           29. A content addressable memory according to claim  
2           28, wherein said first plurality of content addressable  
3           memory cells of a respective storage region is configured  
4           to compare contents stored therein with a key supplied  
5           thereto, and to selectively read out contents of said  
6           second plurality of content addressable memory cells of  
7           said respective storage region in accordance with whether  
8           or not there is a match between contents of said first  
9           plurality of content addressable memory cells and said key.

1           30. A content addressable memory according to claim  
2           29, wherein each of said plurality of storage regions is  
3           further configured to compare contents stored therein with  
4           said read out contents of said second plurality of content  
5           addressable memory cells to determine whether any other of  
6           said plurality of storage regions contains said common  
7           second field.

1           31. A content addressable memory according to claim  
2       28, wherein a respective one of said second plurality of  
3       content addressable memory cells comprises a data bit  
4       storage cell having a data input through which a data bit  
5       is written into said data bit storage cell, a data output  
6       through which a data bit is read out of said data bit  
7       storage cell, and an address input through which said data  
8       bit storage cell is selectively accessed, and a data bit  
9       comparator coupled to said data bit storage cell and being  
10      configured to determine whether the data bit stored in said  
11      data bit storage cell matches a reference data bit during  
12      a read cycle for said data bit storage cell.